Simulation Models for Robust Design Using Location Depth Methods

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Summary

For a cost-effective production of integrated circuits, one important aspect is the accurate simulation of electronic circuits with regard to process variation. Process variation is described as the range of simulation (SPICE) parameters, but to reduce the costs of simulation they are replaced by easy available e-test parameters. An approximate algorithm for the location depth (multivariate ranking) selects all data points with location depth one as boundary points for the multidimensional data set of e-test parameters. The corresponding SPICE parameter values are simply obtained by a linear mapping. To increase the robustness of the simulation the region covered by the set of boundary points is extended by determining the point with deepest location (multivariate median) and adding to each boundary vector a fixed portion of the vector from the median to the boundary vector. This natural extension covers also moderate process shifts without changing the covariance structure of the data. These methods are integrated into an automated generation flow to be applicable in a production and circuit design environment. The statistical methods are validated by simulation experiments of typical analog/mixed-signal circuit designs.

KEY WORDS: location depth, semiconductor industry, boundary wafers, process variation, SPICE, simulation, statistical corner models, robust design

1 Introduction

1.1 General Overview

Today, integrated circuits or microchips play a very important role as heart of electronic devices. Accurate computer simulations during the development of complex chip designs help to avoid cost-intensive iterations of the production. The basis for the simulation of electronic circuits is a precise characterization and modeling of the electronic devices like MOS transistors, resistors or capacitors. Another important aspect in estimating the robustness of a design is process variation. The behaviour of the devices on the chip depends on the setting of the production equipment, and the sensitivity of the design with respect to process fluctuations determines the overall yield (i.e. the number of good chips in a lot).

Thus, several simulation runs have to be performed for one circuit to cover the process variation investigated by two widely used methods: worst case and Monte Carlo simulation. Owing to the small number of simulation points, worst case methods are relatively fast but usually do not reflect the process variation properly. In general, they are too conservative, i.e. good working circuits will not be accepted. The consequences are unnecessary costs for the modification of the design and loss of performance (especially increasing power consumption and chip area). In contrast to worst case simulation, Monte Carlo methods may yield better simulation results, but they demand several hundred simulation runs (i.e. several hours of computing time).

Here we present an alternate framework worked out in the PhD thesis of Kocher [1]. Boundary points are selected by a multivariate ranking procedure and extended by a boundary extension method to cover the process variation appropriately. It produces reliable results even with a small number of boundary points and it is suitable also for high dimensions in contrast to the density estimation procedure proposed in [2]. In other words we establish a modified simulation setup which has a remarkable feature: it produces reliable results in short time.

1.2 Problem Description

The models of the devices used for the simulation of integrated circuits are represented by a set of *simulation (SPICE) parameters* determined from current and voltage measurements of the devices on a sample wafer. Owing to the large number of measurements necessary to obtain reliable parameters, parameter extraction for MOS transistors in an industry-standard device model like BSIM3V3 [3] (approx. 150 parameters) is a very time-consuming task.

We denote the set of SPICE parameters by $P_s = \left\{p_s^{(1)}, \ldots, p_s^{(k)}\right\}$ and a single parameter is given by $p_s \in P_s$. Let $\mathbf{v} \in \mathcal{R}^k$ be a parameter vector with components $v(p_s)^{(j)}, j = 1, \ldots, k$. The values of a single parameter p_s for a certain wafer w are called $v(w, p_s)$, the SPICE parameter vector for wafer w is defined as $\mathbf{v}(w) = \left(v(w, p_s^{(1)}), \ldots, v(w, p_s^{(k)})\right)$, and the devices of several wafers $w_1, \ldots, w_r$ are given by a set of vectors $S = \{\mathbf{v_1}, \ldots, \mathbf{v_r}\}$, where $\mathbf{v_i} = \mathbf{v}(w_i)$. This set S is called *simulation setup*. Our task is to find r boundary vectors (*process corners*) in the SPICE parameter space , i.e. a set $S = \{\mathbf{v_1}, \ldots, \mathbf{v_r}\}$ with $|S| = r$ representing the variation of the process.

2 Data Analysis

A possible approach for a simulation setup S is to determine the SPICE parameters of many ($n > 100$) wafers by parameter extraction and to find $r \ll n$ boundary points in the space of the SPICE parameters (see [4]). However, the extraction of SPICE parameters is a very time-consuming and resource intensive task. For that reason it may not be feasible in a production environment.

To avoid the extraction of many wafers, *production control parameters* (*e-test parameters*) are used to find r wafers representing the process corners. E-test parameters have two important features: (i) they are measured during production for each wafer and (ii) they are easily available. For the simulation, however, they cannot be used directly since e-test parameters are computed by simplified equations. We denote the set of e-test parameters by $P_e = \left\{p_e^{(1)}, \ldots, p_e^{(m)}\right\}$ and a single parameter is given by $p_e \in P_e$. Let $\mathbf{t} \in \mathcal{R}^m$ be a parameter vector with components $t(p_e)^{(i)}$, $i = 1, \ldots, m$. The value of p_e for a certain wafer w is denoted by $t(w, p_e)$, and for wafer w we have the vector $\mathbf{t}(w) = \left(t(w, p_e^{(1)}), \ldots, t(w, p_e^{(m)})\right)$.

The commercial parameter extraction tool IC- CAP^{TM} [4] from Agilent uses this approach. It selects wafers (i.e. process corners) in the e-test parameter space by a non-parametric density estimation method and extracts only the SPICE parameters of the selected wafers, but this number ($r > 10$) is still too large for complete parameter extraction based extensive measurements.

2.1 Our Approach of Data Transformation

We tackle this problem by a different approach. First, the process corners are identified by the boundary points of e-test parameter vectors (see Section 2.2). Second, SPICE parameter values for these wafers are determined by transforming the e-test parameter values. For this method, extracted SPICE parameter values of only one typical wafer (golden wafer) have to be available.

2.1.1 Transformation of e-test parameters to SPICE parameters

In the following we define a (linear) function $e2SPICE : \mathcal{R}^m \rightarrow \mathcal{R}^k$ with $\mathcal{R}^m$ being the space of the e-test parameters and $\mathcal{R}^k$ the space of the SPICE parameters.

A typical wafer w_t is selected and its SPICE parameters are extracted. To find approximate values for the SPICE parameters of another wafer w, the deviation of the corresponding e-test parameter values of wafer w with respect to the values of the typical wafer w_t is used.

Depending on the type of the e-test parameter, two measures of deviation are considered: absolute and relative deviation. The absolute and relative deviation of an e-test parameter p_e can be written as

$$d_{abs}(w, w_t, p_e) = t(w, p_e) - t(w_t, p_e)\,, \quad d_{rel}(w, w_t, p_e) = \frac{t(w, p_e)}{t(w_t, p_e)}.$$

Analogously, for SPICE parameters we have

$$d_{abs}(w, w_t, p_s) = v(w, p_s) - v(w_t, p_s)\,, \quad d_{rel}(w, w_t, p_s) = \frac{v(w, p_s)}{v(w_t, p_s)}.$$

Setting $d_{abs}(w, w_t, p_s) \doteq d_{abs}(w, w_t, p_e)$ resp. $d_{rel}(w, w_t, p_s) \doteq d_{rel}(w, w_t, p_e)$ we get SPICE parameter values in case of the absolute deviation

$$v(w, p_s) = t(w, p_e) + (v(w_t, p_s) - t(w_t, p_e)) \tag{1}$$

and in case of the relative deviation

$$v(w, p_s) = \frac{v(w_t, p_s)}{t(w_t, p_e)}\, t(w, p_e). \tag{2}$$

The transformations (1) and (2), $e2SPICE$, can be written as a linear mapping

$$\mathbf{v} = A \cdot \mathbf{t} + \mathbf{b} \tag{3}$$

where $\mathbf{v}$ is the k-dimensional vector of SPICE parameter values and $\mathbf{t}$ the m-dimensional vector of e-test parameter values ($k \geq m$). Matrix A is of dimension $k \times m$ and vector $\mathbf{b}$ has k elements. The elements of matrix A and vector $\mathbf{b}$ are determined by equations (1) and (2). The SPICE parameter $p_s^{(i)} \in P_s = \left\{p_s^{(1)}, \ldots, p_s^{(k)}\right\}$ corresponds to the i-th row of matrix A and the i-th element of vector $\mathbf{b}$; the e-test parameter $p_e^{(j)} \in P_e = \left\{p_e^{(1)}, \ldots, p_e^{(m)}\right\}$ corresponds to the j-th column of matrix A. Furthermore, for every SPICE parameter $p_s^{(i)}$ there exists a corresponding e-test parameter $p_e^{(j)} \doteq p_s^{(i)}$ whose variation determines the variation of $p_s^{(i)}$. Therefore, the elements a_{ij} of matrix A can be written as

$$a_{ij} = \begin{cases} 1 & p_e^{(j)} \doteq p_s^{(i)}, \text{ abs. deviation} \\ \frac{v(w_t, p_s^{(i)})}{t(w_t, p_e^{(j)})} & p_e^{(j)} \doteq p_s^{(i)}, \text{ rel. deviation} \\ 0 & \text{otherwise}\,, \end{cases} \tag{4}$$

and the elements of vector $\mathbf{b}$ are given as

$$b_i = \begin{cases} v(w_t, p_s^{(i)}) - t(w_t, p_e^{(j)}) & p_e^{(j)} \doteq p_s^{(i)}, \text{ abs. deviation} \\ 0 & \text{otherwise}\,. \end{cases} \tag{5}$$

2.1.2 Verification

For verifying the transformation we simulated a CMOS ring oscillator with several sets of SPICE parameters generated by $e2SPICE$ (3). In this setting $k = 16$ SPICE parameters have been determined from $m = 14$ e-test parameters and applied to 2 different devices (NMOS and PMOS transistors).

The 41-stage ring oscillator was implemented as a process monitor structure in a standard $0.8\mu m$ CMOS process. Simulation results for $n = 48$ wafers from 3 different lots have been compared to the corresponding measurement data (Figure 1). The wafers were taken from three R&D lots where lot 1 and lot 2 had slight problems during production, but the third lot ran already stable. In the third lot even the applied process-split is closely followed by the circuit simulation. The comparison of simulated and measured data indicates that the results of the measurement are reproduced with sufficient accuracy.

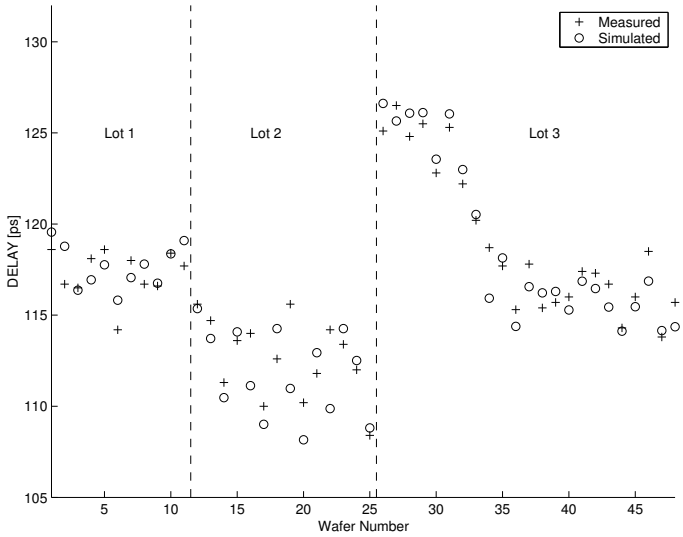

Figure 1: Verification of transformation $e2SPICE$: Ring-Oscillator Delay.

2.2 Statistical Methods

2.2.1 Worst Case Method

Worst case methods are a conventional way to consider process variation. In standard worst case methods the *one-dimensional* e-test parameter limits are combined in a certain way, e.g. for a worst case power corner (highest power consumption) the *minimal effective channel length* and the *maximal effective channel width* parameters are used. In this way a set of e-test parameter values is generated and transformed by $e2SPICE$ (3). The drawback of this method, however, is that correlations between device parameters may be ignored.

2.2.2 The Boundary Method

The boundary method selects boundary points in the e-test parameter space by using a multivariate ranking procedure due to Rousseeuw and Struyf [5] and obtains the corresponding SPICE parameter values by transformation *e2SPICE* (3). The measure for multivariate ranking is the *location depth* where the location depth of an arbitrary point $\boldsymbol{\theta} = (\theta_1, \ldots, \theta_p) \in \mathcal{R}^p$ relative to a p-dimensional data set $Z = \{\mathbf{x_i} = (x_{i1}, \ldots, x_{ip}) | i = 1, \ldots, n\}$ is defined as the smallest number of data points in any closed halfspace with boundary through $\boldsymbol{\theta}$ and can be written as

$$ldepth(\boldsymbol{\theta}; Z) = \min_{||\mathbf{u}||=1} \#\{i | \mathbf{u}^T \mathbf{x_i} \geq \mathbf{u}^T \boldsymbol{\theta}\}\,. \tag{6}$$

An important property of the location depth is the affine invariance, i.e. if $\boldsymbol{\theta}$ is transformed to $A\boldsymbol{\theta} + \mathbf{b}$ with $\mathbf{b} \in \mathcal{R}^p$ and $A \in \mathcal{R}^{p \times p}$ nonsingular then $ldepth(A\boldsymbol{\theta} + \mathbf{b}; AZ + \mathbf{b}) = ldepth(\boldsymbol{\theta}; Z)$.

To visualize this concept by a simple example, the location depth has been computed for a sample of $n = 200$ pairs of independent N(0,1) distributed random variables. In Figure 2 the $r = 12$ points with location depth equal to one are selected as corner points and the convex hull of these 12 points is drawn.

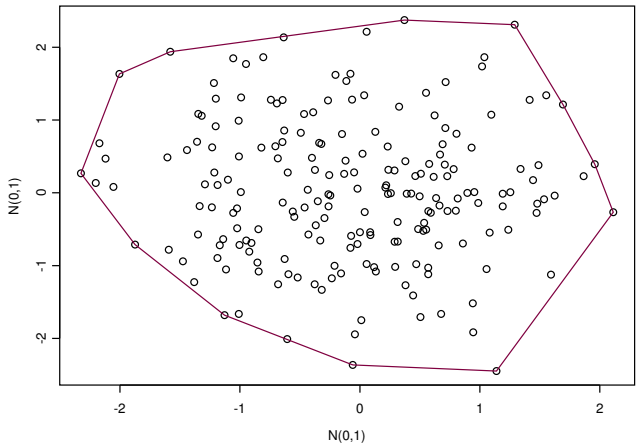

Figure 2: Location Depth Method: Scatter plot of 200 samples of two independent N(0,1) distributed random variables and convex hull of points with $ld_i = 1$.

We now use the location depth to determine boundary wafers out of n wafers $w_1, \ldots, w_n$ with e-test parameter vectors $\mathbf{t}(w_1), \ldots, \mathbf{t}(w_n)$. The m-dimensional data set is defined as $T = \{\mathbf{t}(w_i) | i = 1, \ldots, n\}$ and the location depth ld_i of an e-test parameter vector $\mathbf{t}(w_i)$ can be computed as

$$ld_i = ldepth(\mathbf{t}(w_i), T),\ i = 1, \ldots, n\,. \tag{7}$$

According to the definition of the location depth, e-test parameter vectors on the boundary have value $ld_i = 1$. For that reason, we define the set of wafers on the boundary as

$$W_b = \{w_i \mid ld_i = 1\}\ . \tag{8}$$

The corresponding set of SPICE parameter vectors can be written as

$$S = \{e2SPICE(\mathbf{t}(w_i)) \mid w \in W_b\} = \{A \cdot \mathbf{t}(w_i) + \mathbf{b} \mid w \in W_b\}\ . \tag{9}$$

2.2.3 The Boundary Extension Method

To increase the reliability of the simulation a setup S_{ext} should also cover possible process shifts during production. For this we introduce a method which extends the region in the e-test parameter space.

The Boundary Extension Method uses the set of wafers W_b (8) obtained from the Boundary Method and determines the location center of the data by computing the multivariate median as the point with the highest location depth (*deepest location* due to the algorithm of Struyf and Rousseeuw [6]). Let $\mathbf{t}_{dl}$ be the point (e-test parameter vector) with deepest location.

To enlarge the region covered by the set of boundary wafers W_b (8), directions of decreasing location depth are determined as the vectors from $\mathbf{t}_{dl}$ to the boundary wafers $w \in W_b$:

$$\mathbf{d}_{decr}(w) = \mathbf{t}(w) - \mathbf{t}_{dl}\,. \tag{10}$$

The simulation region is enlarged adding a fixed portion q of $\mathbf{d}_{decr}(w)$ to the e-test parameter vector $\mathbf{t}(w)$. Consequently, we get for all wafers $w \in W_b$ the vectors

$$\mathbf{t}_{ext}(w) = \mathbf{t}(w) + q \cdot \mathbf{d}_{decr}(w) = (1 + q) \cdot \mathbf{t}(w) - q \cdot \mathbf{t}_{dl}\,. \tag{11}$$

In contrast to the vectors $\mathbf{t}(w)$, the generated vectors $\mathbf{t}_{ext}(w)$ do not represent measured parameter values. However, any extended parameter set lies in the electrical neighborhood of a boundary wafer.

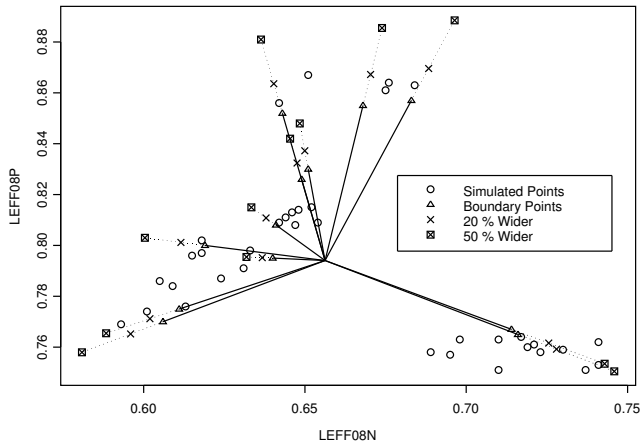

Figure 3: Boundary Extension Method: Scatter plot for the e-test parameters LEFFN and LEFFP (effective channel length for NMOS and PMOS transistor).

The concept of enlarging the simulation region is visualized in Figure 3. The two-dimensional scatter plot shows e-test parameter values for the effective channel length of the NMOS (LEFFN) and PMOS (LEFFP) transistor for the ring oscillator data set (see Section 2.1.2). The circles and triangles represent $n = 48$ data points, where the triangles indicate the values of $r = 12$ boundary wafers $w \in W_b$ obtained from e-test parameter vectors of dimension 14. Figure 3 exhibits the two-dimensional projection to the parameters LEFFN and LEFFP. The solid lines show the directions of decreasing location depth $\mathbf{d}_{decr}(w)$ and the dotted lines represent the extension of the simulation region. The points obtained by enlarging with a portion of $q = 0.2$ are marked with an $\times$, and those for $q = 0.5$ are signified by an $\times$ in a square.

The simulation setup S_{ext} is defined similar to S in (9):

$$\begin{aligned} S_{ext} &= \{e2SPICE(\mathbf{t}_{ext}(w)) \mid w \in W_b\} \\ &= \{(1+q) \cdot A \cdot \mathbf{t}(w) - q \cdot A \cdot \mathbf{t}_{dl} \mid w \in W_b\} \ . \end{aligned} \tag{12}$$

3 Implementation

To obtain models for commercial simulation tools, the Boundary and the Boundary Extension Method are integrated into a generation flow (see Figure 4). As input data the e-test parameter vectors and the SPICE parameter vectors of the typical wafer w_t are needed. The two main parts of the generation flow are the data manipulation with the statistical software package S-PLUS^{TM} [7] and the generation of the libraries with the UNIX shell script PARMGR, developed by *austriamicrosystems AG*.

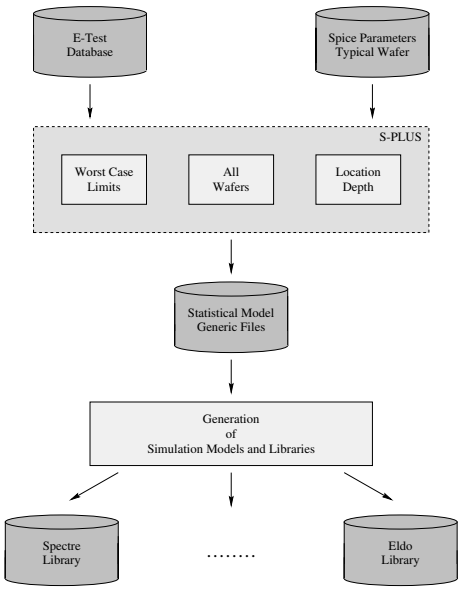

Figure 4: Automated generation flow for Statistical Simulation Models.

The software package S-PLUS is used as data analysis tool where either the Boundary Method or the Boundary Extension Method is applied to the imported data. The resulting simulation setup S (9) resp. S_{ext} (13) is written to a generic model file. The data from the generic model files is then used by the UNIX shell script PARMGR to generate the simulation model libraries for several different analog simulators (e.g. Spectre^{TM}, ELDO^{TM}, HSPICE^{TM}, etc.).

These simulation model libraries allow for typical standard simulations. After defining the necessary performance outputs, the process corner simulation is started and the performance spread due to the process variation can be analyzed.

4 Results

The generation flow for simulation models has been applied to the CMOS ring oscillator data described in Section 2.1.2.

We established, (i) the models for all wafers, (ii) the models for the standard worst cases based on the e-test data limits and (iii) the models of the Boundary Method. With these three models, the ring oscillator circuit was simulated and the corresponding results are presented in Figure 5. The distribution of the delay time of all $n = 48$ wafers are displayed as histogram, whereas the dashed lines (wide limits) represent the Worst Case limits and the solid lines give the close limits of the Boundary Method. Here, the Worst Case Method creates an unrealistic spread of the delay due to the independent combination of the extreme one-dimensional parameter values, whereas the Boundary Method maps the spread of the performance output.

A second set of simulation runs — again for the ring oscillator circuit — was generated to study the behaviour of the Boundary Extension Method in more detail. The extensions are computed for five different portions q ($q \in \{0.1, 0.2, 0.3, 0.4, 0.5\}$). The results can be observed in Figure 6 as lines along with the histogram bars for all 48 wafers. The parameter

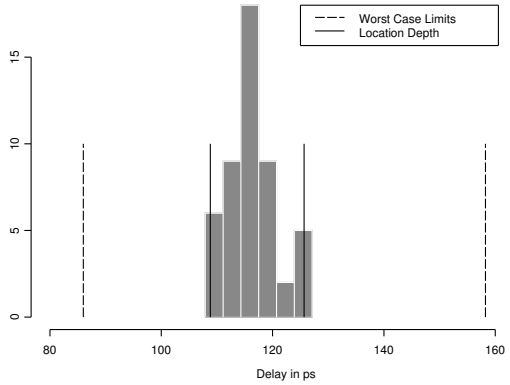

Figure 5: Simulation results for CMOS ring oscillator delay: Location Depth Method vs. Standard Worst Case limits.

values obtained can be used to create more robust designs whose performance outputs lying still within a realistic range.

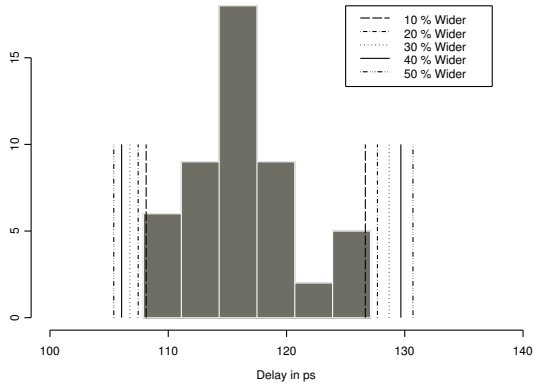

Figure 6: Simulation results for CMOS ring oscillator delay: Extension of the boundaries.

5 Conclusion

In this article, we proposed two methods to find a set of e- test parameter vectors representing the variation of a semiconductor production process. With the Boundary Method, e-test parameter vectors of sampled wafers are determined whereas with the Boundary Extension Method, vectors are generated with the directions of decreasing location depth. The e-test parameter vectors are then transformed by the linear function $e2SPICE$ (3) to the corresponding SPICE parameter vectors.

With our methods, it becomes possible to perform fast and realistic simulations of circuit performance variation. The SPICE parameters have to be extracted only for one wafer (the typical wafer), and a set of simulation parameters is determined from e-test data which is continuously available during production. Therefore, a regular update of the simulation parameters following the actual states of the process can easily be done.

Simulation setups for a ring oscillator yielded proper results using $r = 10$ corner wafers out of $n = 48$ wafers. Kocher [1] studied also operational amplifiers as analog applications based on samples of $n = 512$ ($n = 886$) wafers. He found that models with $r = 17$ ($r = 37$) corner wafers and extension $q = 0.5$ could cover the process variation appropriately. With our new tool, the designer of electronic circuits is now in the position to check the designed circuit for sensitivity to process variations without a need for adjusting it to unrealistic and misleading worst case limits.

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Biographies

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Michael Kocher received his degree as graduate engineer in Technical Mathematics from the Graz University of Technology in 2000. He has been working as process characterization engineer at *austriamicrosystems AG*, Unterpremstätten, Austria from 2001 to 2002. His research was concentrated on the statistical corner modeling of semiconductor devices and design-framework implementation. 2002 he finished his Ph.D. degree in Technical Sciences at the Institute of Statistics, TUG and is at present working as a statistician at *Standard Life* in Frankfurt/Main, Germany.

Gerhard Rappitsch received his degree as graduate engineer in Technical Mathematics from the Graz University of Technology (TUG) in 1991 and in 1996 his Ph.D. degree in Technical Sciences from the same university. From 1992 to 1996 he was with the Austrian Science Fund and member of

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