Robust Design of Electronic Circuits by Location Depth Methods

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1 Goal

Cost-effective production of integrated circuits by accurate simulation of electronic circuits with regard to process variation.

1.1 Approach

The models of the devices are represented by a set of *simulation (SPICE) parameters* determined from current and voltage measurements of the devices on a typical (golden) wafer.

- Model (SPICE) parameters are determined by optimization
- Parameter extraction for MOS transistors in an industry-standard device model like BSIM3V3 (approx. 150 parameters) is very time-consuming

To avoid the extraction of many wafers, *production control (e-test) parameters* are used to find r wafers representing the process corners.

- Production control (e-test) parameters are simplified versions of SPICE parameters
- E-test parameters are measured on each wafer during production
- They are easy available and used for yield analysis

Approximate values for SPICE parameters of wafer w obtained by measuring the deviation of the e-test parameter values of wafer w from the values of the typical wafer w_t. The transformations can be written as linear mapping

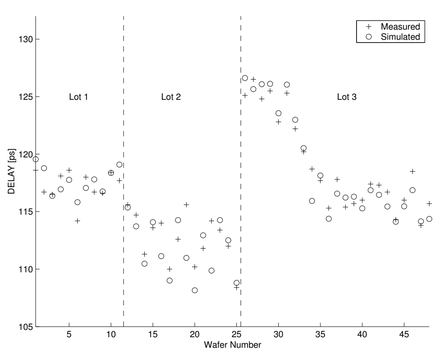
$$\mathbf{v} = A \cdot \mathbf{t} + \mathbf{b}\,. \tag{1}$$

$\mathbf{v}$ k-dimensional vector of SPICE parameter values, $\mathbf{t}$ m-dimensional vector of e-test parameter values ($k \geq m$). $k \times m$ matrix A , k-dimensional vector $\mathbf{b}$.

1.2 Verification

Simulation of a CMOS ring oscillator with several sets of SPICE parameters generated by (1).

- $k = 16$ SPICE parameters, $m = 14$ e-test parameters applied to NMOS and PMOS transistors
- Simulation results for $n = 48$ wafers from 3 different lots are compared to measurements
- Wafers are from three R&D lots: lot 1 and lot 2 had slight problems during production
- Lot 3 was stable and the process-split is closely followed by the circuit simulation



Verification of transformation: ring oscillator delay

2 Statistical Methods

2.1 The Boundary Method

Selection of boundary points in e-test parameter space by multivariate ranking procedure, transformed to SPICE parameter values by (1). Measure for multivariate ranking is *location depth*:

The location depth of an arbitrary point $\boldsymbol{\theta} = (\theta_1, \ldots, \theta_p) \in \mathcal{R}^p$ relative to a p-dimensional data set $Z = \{\mathbf{x_i} = (x_{i1}, \ldots, x_{ip}) | i = 1, \ldots, n\}$ is given as

$$ldepth(\boldsymbol{\theta}; Z) = \min_{||\mathbf{u}||=1} \#\{i | \mathbf{u}^T \mathbf{x_i} \geq \mathbf{u}^T \boldsymbol{\theta}\} \tag{2}$$

where $\mathbf{u}$ ranges over all vectors in $\mathcal{R}^p$ with $||\mathbf{u}|| = 1$.

Property of affine invariance (Donoho and Gasko, 1992, Lemma 2.1):

$$ldepth(A\boldsymbol{\theta} + \mathbf{b}; AZ + \mathbf{b}) = ldepth(\boldsymbol{\theta}; Z)\,.$$

Approximate algorithm of Rousseeuw and Struyf (1998) in $O(mp^3 + mpn)$ time, where $m\ (\leq 50)$ is number of p-subsets used.

m-dimensional data set $T = \{\mathbf{t}(w_i) | i = 1, \ldots, n\}$, location depth ld_i of e-test parameter vector $\mathbf{t}(w_i)$:

$$ld_i = ldepth(\mathbf{t}(w_i), T),\ i = 1, \ldots, n\,. \tag{3}$$

Set of wafers on the boundary

$$W_b = \{w_i \mid ld_i \leq 1\}\ . \tag{4}$$

Corresponding set of SPICE parameter vectors

$$S = \{A \cdot \mathbf{t}(w_i) + \mathbf{b} \mid w \in W_b\}\ . \tag{5}$$

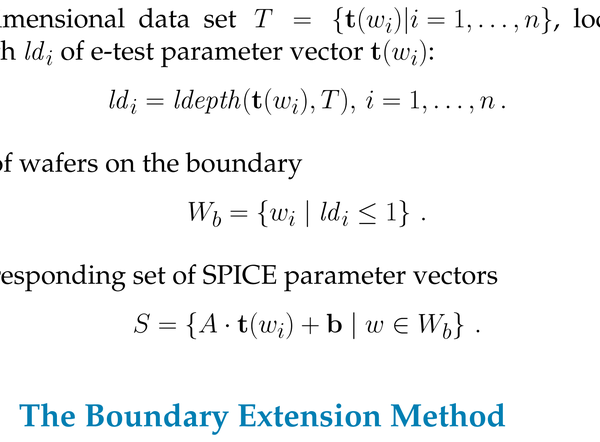
2.2 The Boundary Extension Method

Let $\mathbf{t}_{dl}$ be the point (e-test parameter vector) with deepest location.

$$\mathbf{d}_{decr}(w) = \mathbf{t}(w) - \mathbf{t}_{dl}\,. \tag{6}$$

We get for all wafers $w \in W_b$ the vectors

$$\mathbf{t}_{ext}(w) = \mathbf{t}(w) + q \cdot \mathbf{d}_{decr}(w) = (1 + q) \cdot \mathbf{t}(w) - q \cdot \mathbf{t}_{dl}\,. \tag{7}$$



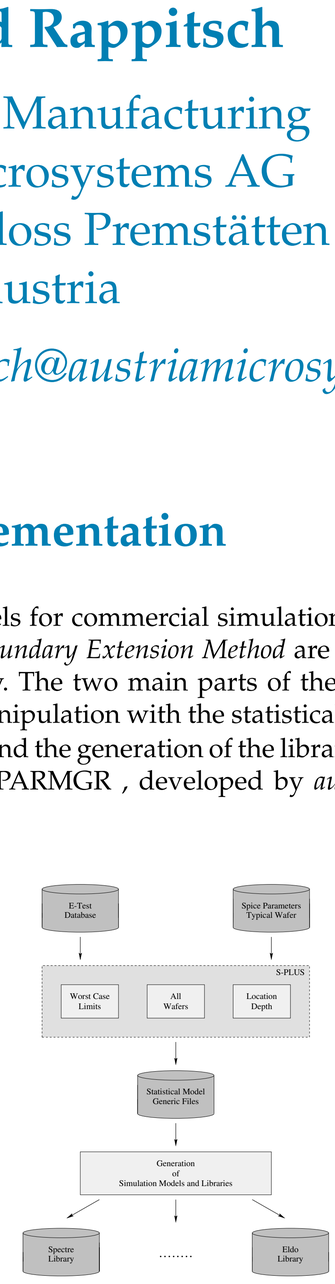
Scatter plot for the e-test parameters LEFFN and LEFFP (effective channel length for NMOS and PMOS transistor)

The simulation setup S_{ext} is defined similar to S in (5):

$$S_{ext} = \{(1 + q) \cdot A \cdot \mathbf{t}(w) - q \cdot A \cdot \mathbf{t}_{dl} \mid w \in W_b\}\ . \tag{8}$$

3 Implementation

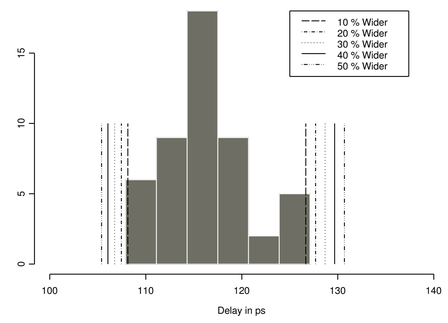
To obtain models for commercial simulation tools, the *Boundary* and the *Boundary Extension Method* are integrated into a generation flow. The two main parts of the generation flow are the data manipulation with the statistical software package S-PLUS^{TM} and the generation of the libraries with the UNIX shell script PARMGR , developed by *austriamicrosystems AG*.



Automated generation flow for Statistical Simulation Models

4 Results

A set of simulation runs for the ring oscillator circuit was generated to study the behavior of the Boundary Extension Method in more detail. The extensions are computed for five different portions q ($q \in \{0.1, 0.2, 0.3, 0.4, 0.5\}$). The results can be observed in the following Figure as lines along with the histogram bars for all 48 wafers. The parameter values obtained can be used to create more robust designs whose performance outputs are still within a realistic range.



Simulation results for CMOS ring oscillator delay: Extension of the boundaries

5 Conclusion

- Fast and reliable nonparametric method based on few wafers
- SPICE models for realistic coverage of process variation: corner wafers and deepest wafer
- Automated generation possible
- **Critical.** Verification of linear mapping
- **Applicable Range.** Stable process, several month after full process release
- Patent from July 20, 2004

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