SPICE Modeling of Process Variation Using Location Depth Corner Models

Gerhard Rappitsch, Ehrenfried Seebacher, Michael Kocher and Ernst Stadlober

Abstract— **For robust designs the influence of process variations has to be considered during circuit simulation. We propose a nonparametric statistical method to find sets of simulation parameters that cover the process spread with a minimum number of simulation runs. Process corners are determined from e-test parameter vectors using a location depth algorithm. The e-test corner vectors are then transformed to SPICE parameter vectors by a linear mapping. A special corner extension algorithm makes the resulting simulation setup robust against moderate process shifts while preserving the underlying correlation structure. To be applicable in a production and circuit design environment, the models are integrated into an automated model generation flow for usage within a design-framework. The statistical methods are validated for analog/mixed-signal benchmark circuits.**

Keywords— **Location Depth, SPICE, Simulation, Statistical Corner Models, Robust Design, Process Variation.**

I. Introduction

DURING the past years, circuit simulation has become more and more important for the development of integrated circuits. The growing complexity of the applications and shorter product development cycles demand high efforts from the designers to create complex designs more quickly. Circuit simulation has become a very important tool to check the functionality of a design before prototyping in order to avoid time-intensive and therefore expensive production iterations.

Besides the precise SPICE modeling of typical semiconductor devices additional aspects of circuit simulation have to be taken into account. For the design of robust circuits, one aspect is the accurate modeling of the process variation and its inclusion within silicon foundry simulation libraries. There exist two standard approaches for analyzing process variation: worst case methods and Monte Carlo methods. The widely used worst case method combines device parameters to maximize a single device performance (e.g. speed, power or voltage levels, see also Section III-A) and provides a fast simulation technique (only a few simulation runs are necessary). Since correlations are usually not taken into account properly, the results may often be too pessimistic. As a consequence, valid designs may be rejected or have to be adjusted to meet artificial and inaccurate worst case limits. This can lead to unnecessarily large chip area and power consumption as well as increasing design efforts and costs.

To obtain more adequate simulations, parametric Monte Carlo methods may be used where the crucial SPICE model parameters are sampled from a pre-defined distribution conforming to the process specification. The problem of Monte Carlo simulations, however, is that hundreds of simulation runs have to be performed and depending on the complexity of analog/mixed-signal circuits this may take several simulation hours to be completed. Parametric Monte Carlo models from production control data (e-test data) are presented in [1] and [2]. Moreover, yield analysis and yield optimization tools based on parametric statistical models are described in [3], [4], [5] and [6]. As far as Monte Carlo models are concerned, the underlying assumptions for parametric models (e.g. normally distributed data) may not be valid for real e-test data.

Recently, nonparametric statistical methods have been employed to establish boundary vectors in worst case models ([7], [8]). The approach introduced in [7] is based on nonparametric density estimation where points with low density values are selected as boundary points in device model generation. The method is usable for generating multivariate SPICE parameter sets from e-test data. In combination with a spatial diversity algorithm points are selected from the original data cloud and may be used for a process in a controlled and stable state. However, the quality of the density estimator strongly depends on the number of data points in the crucial tail regions. For interesting dimensions ($p > 5$) the data distribution in the tails is in general too scattered to get a reliable density estimation.

Our new procedure, shortly reported in [8], uses a nonparametric statistical method based on multivariate ranking by the so called location depth. Data points with low location depth are selected as corner points and extended by a special boundary extension algorithm. This method has some remarkable features: (i) it produces reliable results even with a small number of corner points, (ii) it is robust against moderate process shifts and (iii) it is applicable also for high dimensions in contrast to the density estimation suggested in [7].

A simple illustration is given in Figure 1 where the data cloud of the two e–test parameters NMOS effective channel length and treshold voltage is covered by 10 corner points on the boundary. This method is implemented using the statistical software package S-PLUS and the statistical models obtained are included into a Cadence/Spectre^{TM} Design Framework.

Section II includes the choice of suitable e-test parameter vectors and their transformation to SPICE parameter vectors. The problem of statistical corner models is tackled in Section III where the appropriate selection of both corner wafers and statistically typical wafers is considered. Section IV is devoted to implementation issues. The accu-

G. Rappitsch, E. Seebacher and M. Kocher are with austriamicrosystems AG, Process and Device Characterisation, E. Stadlober is with the Graz University of Technology, Institute of Statistics.

racy and usefulness of the method within an analog/mixed-signal design environment is validated using digital and analog demonstration circuits in Section V. Our findings are concluded in the final Section VI.

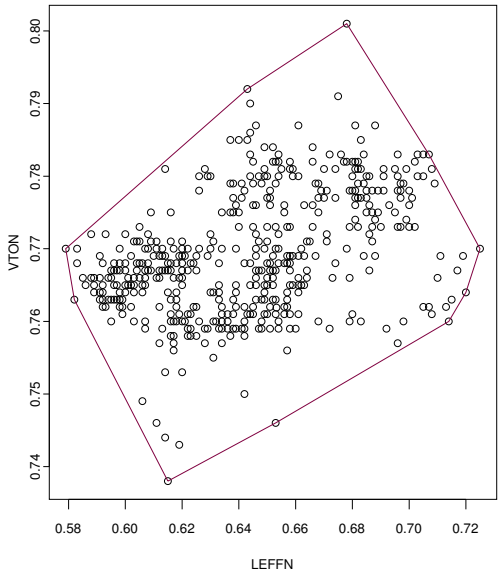


Fig. 1. Scatter plot of LEFFN (NMOS effective channel length) and VTON (NMOS treshold voltage).

II. Transformation of E-Test Parameters to SPICE Parameters

A. SPICE Parameters

The proposed method for the determination of statistical corner models starts with the selection of corner wafers in the e-test parameter space (see Section III). The e-test parameters have to be transformed to SPICE parameters of the device models used. In the subsequent sections the selection of e-test parameters and their transformation to SPICE parameters are explained for NMOS and PMOS transistors and the BSIM3V3 MOS transistor model [9].

To perform the simulation of a circuit, accurate SPICE models of the devices have to be available. The parameters of these models (SPICE parameters) are determined from current and voltage measurements of the devices on a reference wafer by applying optimization methods [10]. Owing to the large number of measurements necessary to obtain reliable parameters, parameter extraction for MOS transistors and an industry-standard device model like BSIM3V3 [9] (approx. $k = 150$ parameters) is very time-consuming.

We denote the set of SPICE parameters by $P_s = \left\{p_s^{(1)}, \ldots, p_s^{(k)}\right\}$ with $|P_s| = k$ the dimensionality of the parameter space and a single parameter by $p_s \in P_s$. A parameter vector is a vector $\boldsymbol{v} \in \mathbb{R}^k$, the value of a single parameter p_s is denoted by $v(p_s)$. Likewise, the values of a single parameter p_s for a certain wafer w are called $v(w, p_s)$ and the SPICE parameter vector for wafer w is defined as $\boldsymbol{v}(w) = \left(v(w, p_s^{(1)}), \ldots, v(w, p_s^{(k)})\right)^T$. Consequently, the devices on a specific wafer are represented by a vector of SPICE parameter values.

A possible approach to find a set of parameter vectors that represent the process variation is to determine the SPICE parameter vectors of many wafers ($n > 100$) by parameter extraction and to find extreme points in the space of the SPICE parameters [11]. The drawback of this method, however, is that the full extraction of SPICE parameters is too expensive to be feasible in a production environment where several processes have to be supported and the characterization has to be updated regularly.

B. E-Test Parameters

To avoid the expensive extraction of several wafers, production control parameters (or e-test parameters) can be used to identify wafers that represent the process corners. For each wafer the production control parameters are measured during production and the values are saved in a database. For simulation purposes, however, they cannot be used directly since e-test parameters are computed by simplified equations to increase the speed of the measurement.

We denote the set of e-test parameters by $P_e = \left\{p_e^{(1)}, \ldots, p_e^{(m)}\right\}$ with $|P_e| = m$ the dimensionality of the e-test parameter space and a single e-test parameter by $p_e \in P_e$. An e-test parameter vector is a vector $\boldsymbol{t} \in \mathbb{R}^m$, the value of a single parameter p_e is denoted by $t(p_e)$. Likewise, the values of an e-test parameter p_e for a certain wafer w are called $t(w, p_e)$ and the e-test parameter vector for wafer w is the vector $\boldsymbol{t}(w) = \left(t(w, p_e^{(1)}), \ldots, t(w, p_e^{(m)})\right)^T$.

The commercial parameter extraction tool IC-CAP^{TM} [11] from Agilent selects wafers representing the process corners by a nonparametric density estimation method in the e-test parameter space and extracts the SPICE parameters of the selected wafers. With this method the number of extracted wafers is reduced, but this number ($r > 10$) is still too large for an efficient extraction and measurement.

C. Parameter Selection and Data Transformation

In our approach the wafers representing the process corners are chosen by a multi-variate ranking method applied to the e-test parameter vectors. Approximations of the corresponding SPICE parameter values are calculated by transforming the e-test parameter values with respect to the SPICE parameters of a single typical wafer (also called 'golden wafer'). With this the exact SPICE parameter values have to be extracted from one typical wafer only and suitable SPICE parameter values of corner wafers are simply obtained from the e-test parameter values. Subsequently we specify the transformation of the e-test parameters to the simulation parameters, i.e. we define a function $e2SPICE : \mathbb{R}^m \to \mathbb{R}^k$ with $\mathbb{R}^m$ being the space of e-test parameters and $\mathbb{R}^k$ the space of SPICE parameters.

For every process a typical wafer w_t is determined and

TABLE I
CORRESPONDING BSIM3V3 (p_s) AND E-TEST PARAMETERS (p_e): TYPE OF VARIATION APPLIED.

p_s	p_e	Type
$vth0$	VTON/P	abs
xw	WEFFN/P	abs
xl	LEFFN/P	abs
tox	TGOXN/P	abs
$u0$	U0N/P	rel
$nsub$	NSUBN/P	abs
nch	NSUBN/P	abs
rsh	RDIFFN/P	abs

the SPICE parameters for all devices of interest are extracted only for this wafer w_t. To find suitable values for the SPICE parameters of another wafer w, the deviation of the corresponding e-test parameter values of wafer w with respect to the typical wafer w_t has to be calculated. This deviation is then equated with the deviation between the SPICE parameters for wafer w and the extracted SPICE parameters for wafer w_t.

In order to analyze the MOS transistor process variation the following $m = 14$ e-test parameters are selected for NMOS and PMOS transistors: VTON and VTOP (treshold voltage for long and wide transistor), LEFFN and LEFFP (effective channel length for a small channel transistor), WEFFN and WEFFP (effective channel width for a narrow channel transistor), TGOXN and TGOXP (gate oxide thickness), U0N and U0P (effective mobility), NSUBN and NSUBP (substrate doping), RDIFFN and RDIFFP (n-diffusion and p-diffusion sheet resistance).

The following $k = 2 \times 8 = 16$ BSIM3V3 parameters were chosen as corresponding SPICE parameters: $vth0$, xl, xw, tox, $u0$, $nsub$, nch, rsh. The correspondence between the selected e-test and BSIM3V3 parameters is shown in Table I.

To generate SPICE parameters for any wafer w the deviation of the corresponding e-test parameter from the typical wafer w_t is applied to the typical SPICE parameter vector $\boldsymbol{v}(w_t)$.

Depending on the type of the e-test parameters, two kinds of deviations are considered: absolute and relative deviation. The absolute deviation of the e-test parameters can be written as

$$d_{abs}(w, w_t, p_e) = t(w, p_e) - t(w_t, p_e) \tag{1}$$

and the relative deviation as

$$d_{rel}(w, w_t, p_e) = \frac{t(w, p_e)}{t(w_t, p_e)}. \tag{2}$$

For the SPICE parameters we have similarly

$$d_{abs}(w, w_t, p_s) = v(w, p_s) - v(w_t, p_s) \tag{3}$$

and

$$d_{rel}(w, w_t, p_s) = \frac{v(w, p_s)}{v(w_t, p_s)}. \tag{4}$$

By equating the absolute deviations $d_{abs}(w, w_t, p_s) = d_{abs}(w, w_t, p_e)$ and the relative deviations $d_{rel}(w, w_t, p_s) = d_{rel}(w, w_t, p_e)$ the SPICE parameter value for any wafer is calculated in case of the absolute deviation as

$$v(w, p_s) = t(w, p_e) + (v(w_t, p_s) - t(w_t, p_e)) \tag{5}$$

and for the relative deviation as

$$v(w, p_s) = \frac{v(w_t, p_s)}{t(w_t, p_e)} \cdot t(w, p_e). \tag{6}$$

Owing to the linear structure of the transformation, *e2SPICE* can be written as a linear mapping

$$\boldsymbol{v} = \boldsymbol{A} \cdot \boldsymbol{t} + \boldsymbol{b} \tag{7}$$

where $\boldsymbol{v}$ is the k-dimensional vector of SPICE parameter values and $\boldsymbol{t}$ the m-dimensional vector of e-test parameters ($k \geq m$). The matrix $\boldsymbol{A}$ is of dimension $k \times m$ and vector $\boldsymbol{b}$ has k elements. The elements of matrix $\boldsymbol{A}$ and vector $\boldsymbol{b}$ can be determined by Equations (5) and (6) where the SPICE parameter $p_s^{(i)} \in P_s = \left\{p_s^{(1)}, \ldots, p_s^{(k)}\right\}$ corresponds to the i-th row of matrix $\boldsymbol{A}$ and the i-th element of vector $\boldsymbol{b}$, and the e-test parameter $p_e^{(j)} \in P_e = \left\{p_e^{(1)}, \ldots, p_e^{(m)}\right\}$ corresponds to the j-th column of matrix $\boldsymbol{A}$. Furthermore, for every SPICE parameter $p_s^{(i)}$ there is a corresponding e-test parameter $p_e^{(j)} = c(p_s^{(i)})$ whose variation is used to determine the variation of $p_s^{(i)}$. Table I shows the type of deviation for all SPICE parameters p_s considered. Therefore, the elements of matrix $\boldsymbol{A}$ are given as

$$a_{ij} = \begin{cases} 1 & p_e^{(j)} = c(p_s^{(i)}), \text{abs. deviation} \\ \frac{v(w_t, p_s^{(i)})}{t(w_t, p_e^{(j)})} & p_e^{(j)} = c(p_s^{(i)}), \text{rel. deviation} \\ 0 & \text{otherwise}, \end{cases} \tag{8}$$

and the elements of vector b read

$$b_i = \begin{cases} v(w_t, p_s^{(i)}) - t(w_t, p_e^{(j)}) & p_e^{(j)} = c(p_s^{(i)}), \\ & \text{abs. deviation} \\ 0 & \text{otherwise}. \end{cases} \tag{9}$$

To verify transformation *e2SPICE* (7) we simulated a CMOS ring oscillator with several sets of SPICE parameters generated by *e2SPICE* for a dataset of $n = 48$ wafers from 3 different lots. For this purpose $k = 16$ SPICE parameters (see Table I) have been determined from $m = 14$ e-test parameters and two devices (NMOS and PMOS transistors).

The 41-stage ring oscillator was implemented as a process control structure (scribe line monitor) in a standard $0.8\mu m$ CMOS process. The simulated results have been compared to the corresponding measurement data (Figure 2) which was available as process control data. The wafers were taken from three R&D lots where lot 2 had slight problems during production. The third lot ran already stable and in this lot also the applied process-split is closely followed by the circuit simulation with a relative error less than 2%. The comparison of simulated and measured data shows that the results of the measurement are reproduced with sufficient accuracy.

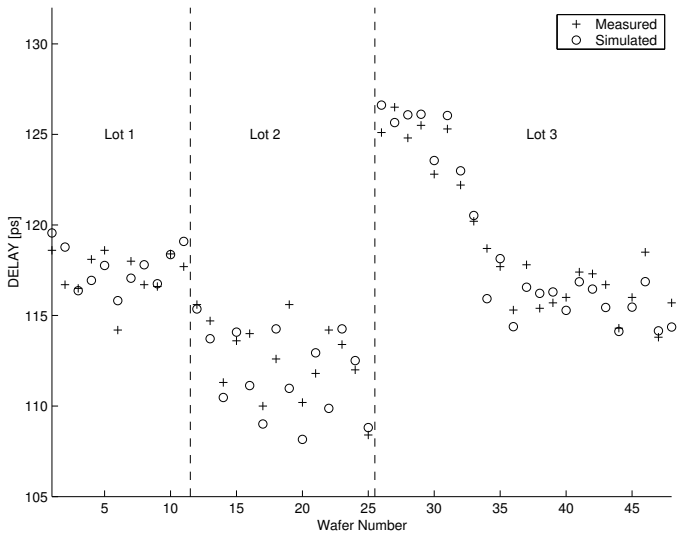


Fig. 2. Verification of transformation *e2SPICE*: Ring-Oscillator Delay.

III. Statistical Corner Models

Transformation *e2SPICE* (7) opens the door to a more efficient procedure. The time-consuming task of extracting SPICE parameter values for all corner wafers (as suggested in [11]) can be replaced by the simple task of transforming e-test parameter vectors to corresponding SPICE parameter vectors by e2SPICE using only the extracted SPICE parameter vector of the typical wafer.

First we shortly describe the conventional worst case method which will be compared with the proposed statistical method. Our statistical method to determine the boundary points in the high-dimensional parameter space is based on an idea called location depth which can be calculated for each data point by the algorithm of Rousseeuw and Struyf [12]. The location depth is a multivariate extension of univariate statistical ranking due to Tukey [13].

In a second step we introduce a procedure which extends the multivariate boundary region by adding a safety margin. With this safety margin, the existing process variation is increased to assure that the checked circuit works also correctly if the process varies more than the underlying data may reflect.

Finally, we describe a method to find a statistically typical wafer, which can be considered as an estimator of the multivariate median. The generation of SPICE parameters for a statistically typical wafer is an important step in creating robust designs since it enables efficient design centering.

A. Standard Worst Case Method

Worst case methods are a usual way to take process variation into account. For standard worst case methods the *one-dimensional* e-test parameter limits (pass/fail limits) are combined to maximize a single device performance: e.g. for a MOS transistor worst case power corner (highest power consumption), the minimal effective channel length, the maximal effective channel width, the minimal threshold voltage and the maximum mobility (gain factor) are set to their extreme values. The principle may be illustrated by assuming a simplified transistor equation for the MOS transistor saturation current:

TABLE II
Spice parameters p_s and analog corners.

$Parameter$	$WorstPower$	Worst Speed
$vth0$	min	max
xw	max	min
xl	min	max
tox	min	max
$u0$	max	min
$nsub$	min	max
nch	min	max
rsh	min	max

$$IDS = \frac{u0\epsilon_{ox}(W + xw)}{tox(L + xl)}\,(VGS - vth0))^2 \qquad (10)$$

with design variables W(drawn width), L(drawn length), VGS (gate-source voltage) and the physical constant ϵ_{ox}. The maximization/minimization of IDS leads to worst case power/worst case speed corners and can be achieved by setting the device parameters to their upper and lower limits as listed in Table II. The maximum and minimum values are calculated from the pass/fail limits of the corresponding e-test parameters (see Table I in Section II-C) which are transformed to the SPICE parameter limits by transformation (7). Within the *austriamicrosystems* design environment four types of worst cases are constructed for MOS transistors: worst case speed (slow NMOS and PMOS) and worst case power (fast NMOS and PMOS) for analog applications (see Table II), as well as worst case one (fast NMOS, slow PMOS) and worst case zero (slow NMOS, fast PMOS) for digital applications. The problem of this method, however, is that existing correlations between device parameters are often ignored leading to pessimistic corner values and hence to large spread during analog simulation of circuit performance. Figure 9 in Section V-A shows negative correlation between oxide thickness TGOXN and substrate doping NSUBN, but for the worst case speed corner the minimization of IDS (10) would rather assume positive correlation: a maximum oxide thickness TGOXN (low gain factor) combined with a maximum substrate doping NSUBN (high effective treshold voltage).

B. Location Depth Corner Method (LDCM)

In contrast to standard worst case methods, the proposed Location Depth Corner method (LDCM) does not use artificial combinations of parameter values. The corner points are determined by the location depth method applied to e-test parameter vectors of real wafers. The key idea of the location depth (Tukey, [13]) is to measure how deep a point lies in the data cloud. For a sample of one-dimensional data

there is a direct correspondence to univariate ranking: minimum and maximum have the lowest location depth (= 1) and the median has the highest location depth (= $\lceil n/2 \rceil$). The formulation of the location depth is valid also in higher dimensions enabling the location of corner wafers represented by a set of e-test parameters ($m > 10$). As described in [12], the location depth of an arbitrary point $\boldsymbol{\theta} = (\theta_1, \ldots, \theta_p) \in \mathbb{R}^p$ relative to a p-dimensional data set $\boldsymbol{Z} = \{\mathbf{x_i} = (x_{i1}, \ldots, x_{ip}); i = 1, \ldots, n\}$ is defined as the smallest number of data points in any closed half-space with boundary through $\boldsymbol{\theta}$ and can be written as

$$ldepth(\boldsymbol{\theta}; \boldsymbol{Z}) = \min_{||\mathbf{u}||=1} \#\{i; \mathbf{u^T x_i} \geq \mathbf{u^T \theta}\} \qquad (11)$$

where $\mathbf{u}$ ranges over all vectors in $\mathbb{R}^p$ with $||\mathbf{u}|| = 1$. A very important property of the location depth is the affine invariance, i.e. if $\boldsymbol{\theta}$ is transformed to $\boldsymbol{A\theta}+\mathbf{b}$ with $\mathbf{b} \in \mathbb{R^P}$ and $\boldsymbol{A} \in \mathbb{R}^{p \times p}$ nonsingular then $ldepth(\boldsymbol{A\theta}+\mathbf{b}; \boldsymbol{AZ}+\mathbf{b}) = ldepth(\boldsymbol{\theta}; \boldsymbol{Z})$. Considering the linear relationship between e-test parameters and SPICE parameters in transformation *e2SPICE* (7) means, that the structure of the multivariate ranking is preserved in the SPICE parameter domain.

Owing to the relation of the location depth in the one-dimensional case $\boldsymbol{z} = (x_1, \ldots, x_n)^T$

$$ldepth(\theta; \boldsymbol{z}) = \min(\#\{i; x_i \leq \theta\}, \#\{i; x_i \geq \theta\}) \qquad (12)$$

to the ranking of the observations $x_{(1)} < \ldots < x_{(n)}$, the location depth is also referred to as multivariate ranking.

An efficient approximate algorithm due to Rousseeuw and Struyf [12] is available for the calculation of the location depth in higher dimensions. It is used to establish the corner points in the proposed LDCM method:

1. Set $ldepth(\boldsymbol{\theta}; \boldsymbol{Z}) \leftarrow n$. $O(1)$
2. Repeat m_d times: $O(m_d)$
   (a) Draw a random sample of size p $O(p)$
   (b) Determine a direction $\mathbf{u}$ perpendicular to the p-subset. $O(p^3)$
   (c) Project all data points on the line L through $\boldsymbol{\theta}$ with direction $\mathbf{u}$. $O(np)$
   (d) Compute the univariate depth k of $\boldsymbol{\theta}$ on L. $O(n)$
   (e) Put $ldepth(\boldsymbol{\theta}; \boldsymbol{Z}) \leftarrow \min(ldepth(\boldsymbol{\theta}; \boldsymbol{Z}), k)$. $O(1)$

The accuracy of the algorithm strongly depends on the number of search directions m_d (see Section V-C).

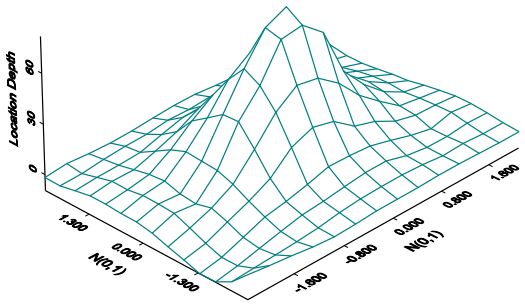


Fig. 3. Location Depth: Surface plot of the location depth for 200 samples of two independent N(0,1) distributed random variables.

To visualize this concept, the location depth has been computed for a sample of $n = 200$ pairs of independent N(0,1) distributed random variables. In Figure 3 the location depth is plotted against the two variables. It can be observed that the lowest values are in the tails and that the maximum is reached in the center. In Figure 4 the points with location depth less equal one are selected ($r = 12$ points) and the convex hull of these 12 points is drawn.

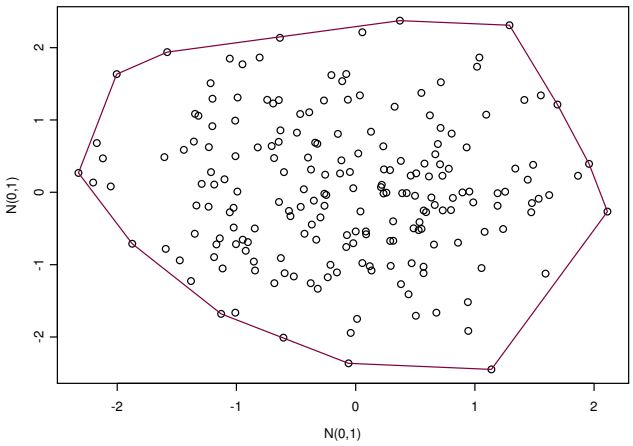


Fig. 4. Location Depth Method: Scatter plot of $n = 200$ samples for two independent N(0,1) distributed random variables and convex hull of points with $ld_i \leq 1$.

This leads us directly to a procedure for determining corner models. The proposed Location Depth Corner Method (LDCM) consists of three computational tasks (see Figure 5): (i) the computation of the location depth based on the e-test parameter vectors, (ii) the choice of the corner wafers as points with location depth less equal 1 and (iii) the transformation *e2SPICE* to generate the SPICE parameter vectors for the corner wafers from the e-test parameter vectors and the typical parameter set.

The original sample consists of n wafers $w_1, \ldots, w_n$ with e-test parameter vectors $\boldsymbol{t}(w_1), \ldots, \boldsymbol{t}(w_n)$. The m-dimensional data set for the location depth is then defined as $\boldsymbol{T} = \{\boldsymbol{t}(w_i) | i = 1, \ldots, n\}$ and the location depth ld_i of an e-test parameter vector $\boldsymbol{t}(w_i)$ can be computed as

$$ld_i = ldepth(\boldsymbol{t}(w_i), \boldsymbol{T}), \; i = 1, \ldots, n. \qquad (13)$$

We select wafers whose location depth is less or equal to one, i.e. we define the set of corner wafers as

$$\boldsymbol{W}_b = \{w_i \mid ld_i \leq 1\}. \qquad (14)$$

The set $\boldsymbol{S}$ of SPICE parameter vectors representing the corner wafers can be written as

$$\begin{aligned} \boldsymbol{S} &= \{e2SPICE(\boldsymbol{t}(w_i)) \mid w \in W_b\} \\ &= \{\boldsymbol{A} \cdot \boldsymbol{t}(w_i) + \boldsymbol{b} \mid w \in W_b\}. \end{aligned} \qquad (15)$$

C. Extended Location Depth Corner Method (ELDCM)

The set $\boldsymbol{S}$ of SPICE parameter vectors (15) resulting from the location depth method is based on e-test parameter values of real wafers. Therefore, by simulating a circuit with the set $\boldsymbol{S}$, the envelope of the process variation based on the underlying data sample is determined.

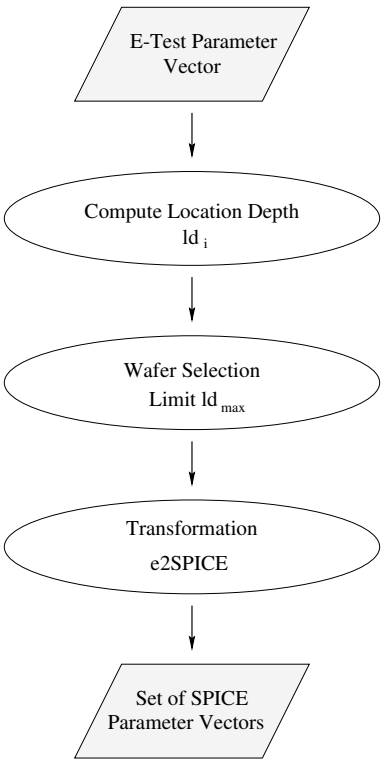


Fig. 5. Steps of the Location Depth Corner Method (LDCM).

To increase the robustness of the simulation setup one has to find another set of SPICE parameter vectors that also covers moderate future process shifts. For that reason we introduce the Extended Location Depth Corner Method (ELDCM) which enlarges the region in the e-test parameter vector space by a certain percentage.

The Extended Location Depth Corner Method, like the LDCM, starts by determining the location depth ld_i of all e-test parameter vectors and selecting the wafers $\boldsymbol{W}_b$ (14) on the boundary. The next step is to search for the center of the data in the e-test parameter space. This search is carried out by the algorithm of Struyf and Rousseeuw [14] which finds the point with largest location depth, denoted as deepest location. By applying the algorithm we establish the deepest location and its corresponding e-test parameter vector $\boldsymbol{t}_{dl}$.

To enlarge the region covered by the boundary wafers $\boldsymbol{W}_b$, directions of decreasing location depth are determined. By direction of decreasing location depth, we denote vectors from the deepest location $\boldsymbol{t}_{dl}$ to the boundary wafers $w \in \boldsymbol{W}_b$:

$$\boldsymbol{d}_{decr}(w) = \boldsymbol{t}(w) - \boldsymbol{t}_{dl}\,. \tag{16}$$

The vectors $\boldsymbol{d}_{decr}(w)$ allow for an enlargement of the simulation region by adding a fixed portion q of $\boldsymbol{d}_{decr}(w)$ to the e-test parameter vector $\boldsymbol{t}(w)$. Consequently, we get

$$\begin{aligned} \boldsymbol{t}_{ext}(w) &= \boldsymbol{t}(w) + q \cdot \boldsymbol{d}_{decr}(w) \\ &= (1+q) \cdot \boldsymbol{t}(w) - q \cdot \boldsymbol{t}_{dl} \end{aligned} \tag{17}$$

as the generated e-test parameter vectors $\boldsymbol{t}_{ext}(w),\ w \in \boldsymbol{W}_b$. In contrast to the vectors $\boldsymbol{t}(w)$, the generated e-test parameter vectors $\boldsymbol{t}_{ext}(w)$ do not represent measured parameter values any more. However, any extended parameter set lies in the electrical neighborhood of a corner wafer and the data envelope is extented in a natural way preserving the original correlation structure.

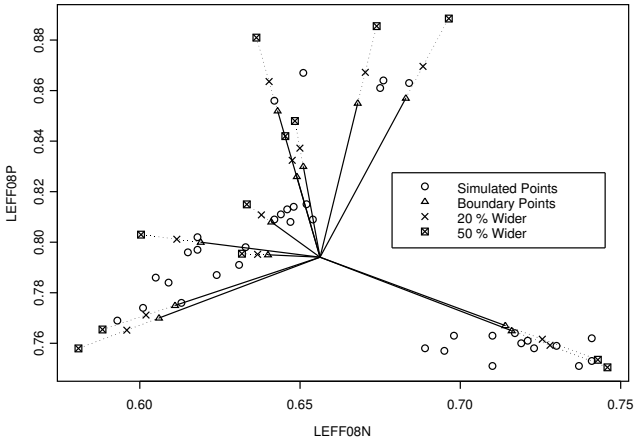


Fig. 6. Boundary Extension Method (ELDCM): Scatter plot for the e-test parameters LEFFN and LEFFP (effective channel length for NMOS and PMOS transistor).

The concept of enlarging the simulation region is visualized in Figure 6. A two-dimensional scatter plot shows the e-test parameter values for the effective channel length of the NMOS (LEFFN) and PMOS (LEFFP) transistor for the ring oscillator data set (see Section II-C). The circles and triangles represent $n = 48$ data points where the triangles indicate the values of $r = 12$ corner wafers $w \in W_b$ resulting from the LDCM method with $m_d = 10$ search directions. Each wafer is characterized by its e-test parameter vector of dimension $m = 14$ and Figure 6 reflects the two-dimensional projection to the parameters LEFFN and LEFFP. The solid lines show the directions of decreasing location depth $\boldsymbol{d}_{decr}(w)$ where the dotted lines represent the extensions of the simulation region. The points obtained when enlarging with a portion of $q = 0.2$ are marked with an $\times$ and those for $q = 0.5$ are signified by an $\times$ in a square. It is obvious that the data cloud is extended without significantly changing the correlation structure.

The e-test parameter vectors $\boldsymbol{t}_{ext}(w), w \in \boldsymbol{W}_b$ are transformed to SPICE parameter vectors by $e2SPICE$ (7) defining the set $\boldsymbol{S}_{ext}$ as

$$\begin{aligned} \boldsymbol{S}_{ext} &= \{e2SPICE(\boldsymbol{t}_{ext}(w)) \mid w \in \boldsymbol{W}_b\} \\ &= \{(1+q) \cdot \boldsymbol{A} \cdot t(w) - q \cdot \boldsymbol{A} \cdot t_{dl} \mid w \in \boldsymbol{W}_b\}\ . \end{aligned} \tag{18}$$

D. Determination of a Statistically Typical Wafer

Whenever a new process is introduced, process limits for the production control parameters are specified. Based on those limits and on the wafers produced during the first months of production, a typical wafer (golden wafer) is selected for parameter extraction such that its parameter

values are near the mean values of a chosen set of key parameters (treshold voltage, oxide thickness, effective channel length, ...). However, for some other parameters not in the set the corresponding values on the golden wafer may be near the pass/fail limits. This can cause problems for the designer in producing a circuit with high yield, because he centers the design only according to the extracted parameter set and some basic design variables. Figure 14 in Section V-C shows an example of a CMOS OpAmp leading to bad yield for the gain bandwidth due to the mobility parameter $u0$ close to the lower limit.

The statistically typical wafer w_{st} is defined as the wafer with the largest location depth (deepest location) in the e-parameter space, i.e. having its parameter vector near to $\boldsymbol{t}_{dl}$, and can be considered as median of the multivariate data set. Let $\boldsymbol{W} = \{w_i \mid i = 1, \ldots, n\}$ be the set of wafers analyzed, then w_{st} denotes the wafer with location depth

$$ld_{st} = \max_{w_i \in \boldsymbol{W}} ld_i \,. \tag{19}$$

A full SPICE parameter set (updated golden wafer extraction) may now be extracted for wafer w_{st} which will improve the quality of the simulation because of a better design centering.

IV. Implementation

A. Parameter Generation and Tool Kit Integration

The techniques described above are now used to define a flow to generate SPICE library files automatically. This flow is shown in Figure 7.

The two essential parts of the generation flow are (i) data manipulation and analysis with the statistical software package S-PLUS^{TM} [15], and (ii) the creation of the libraries by the library generation program PARMGR developed by *austriamicrosystems AG*.

The information about wafer production, i.e. the values of the e-test parameters, are stored in a production database. From this database, values are exported and imported into S-PLUS. Additionally, the extracted SPICE parameter values of the typical wafer are stored in a UNIX/M4-database where they can be exported from. S-PLUS collects all data necessary for calculating the worst case and statistical corner models. The computation includes the selection of appropriate wafers (Location Depth Corner Method), the extension of the simulation region (Extended Location Depth Corner Method), the determination of a statistically typical wafer and the transformation of e-test parameters to SPICE parameters using *e2SPICE* (7). Finally, the model generation information about the SPICE parameters of the wafers is exported to generic data files (*csv*-format).

The generic files are then used by the UNIX parameter generation program PARMGR to generate the simulation model libraries for different analog simulators supported by the foundry (e.g. Spectre^{TM}, ELDO^{TM}, HSPICE^{TM}, etc.).

The simulation models corresponding to the statistical corners are generated automatically from a common database. For integration into the Cadence^{TM} analog/mixed-signal design flow of the *austriamicrosystems AG* design environment (*HIT-Kit*) the models are generated in native Spectre^{TM} format. Each statistical corner is defined as a section in the CMOS model library. Additionally, a corner-definition file (*dcf-file*) is generated which can be loaded into the Cadence Affirma^{TM} [16] corner simulation tool. After performing a standard simulation and defining the necessary performance outputs, the corner simulation is started. For that purpose the *dcf-file* (corner definition file) is loaded and the performance spread due to the process variation can be analyzed graphically.

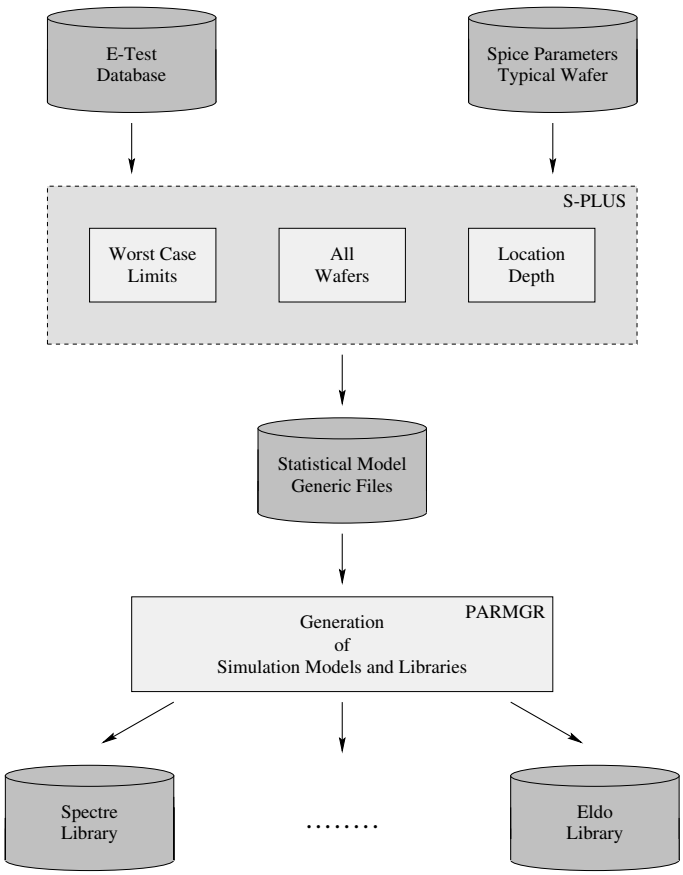


Fig. 7. Automated parameter generation flow for Statistical Corner Models.

V. Verification Results

A. Exploratory Data Analysis

To get a first impression about the distribution of e-test parameters, an exploratory data analysis is performed. First, we examine the one-dimensional distribution of each e-test parameter. Figure 8 shows a typical characteristic (sample size $n = 521$ wafers). The histogram and the density estimation of the effective channel length LEFFN of an NMOS transistor ($0.8\mu m$) indicate non-normal distribution which is supported also by the low p-value ($p = 4.4e^{-7}$) of the Kolmogorov Smirnov test. We note that most other e-test parameters have to be classified as non-normal distributed and thus the statistical methods based on normal

distributional assumptions are not adequate.

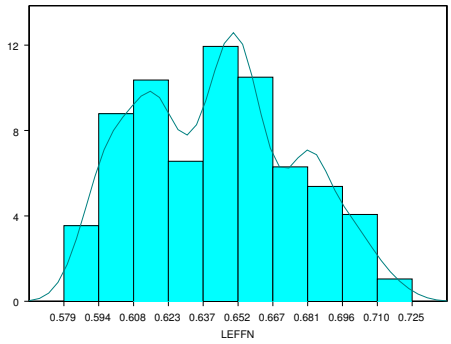


Fig. 8. Histogram with density line for LEFFN.

Another property that is being examined is the correlation structure of the e-test parameters. The standard worst case methods combine one-dimensional e-test parameter limits to get the simulation limits, but do not consider the correlations properly. An example is exhibited in Figure 9. The scatterplot of the substrate doping NSUBN against the gate oxide thickness TGOXN shows some negative correlation, but the standard worst cases (see Table II in Section III) are combined by using the minimum (worst case power) resp. the maximum (worst case speed) parameter values according to the influence of the body effect (substrate doping) on the threshold voltage and on the drain saturation current. Of course, these limits are misleading and do not represent the structure of the data.

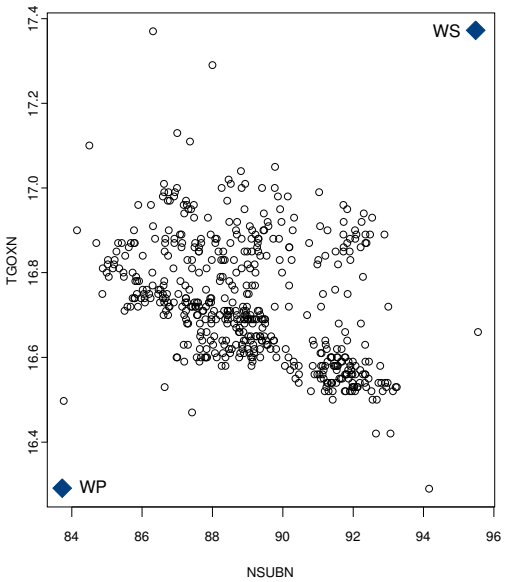


Fig. 9. Scatter plot of NSUBN and TGOXN.

Our location depth approach (LDCM and ELDCM) avoids the problems mentioned above. The proposed methods are nonparametric, i.e. no distributional assumptions of the data are made. Furthermore, by using the e-test parameter vectors of real wafers, no artificial samples are generated and the correlation structure is taken into account.

B. Digital Application - Ring Oscillator Delay

To check the results of the LDCM and the ELDCM on digital circuits, we use the delay data for the CMOS Ring Oscillator introduced in Section II-C to verify the usefulness of the transformation from e-test parameters to SPICE parameters.

The NMOS and PMOS transistors are described by $m = 14$ e-test parameters (see Table I in Section II-C). Applying the LDCM method to a data sample of $n = 48$ wafers, $r = 12$ statistical corners have been identified, and the $k = 16$ SPICE parameters for the BSIM3V3 model were obtained by transformation e2SPICE (7).

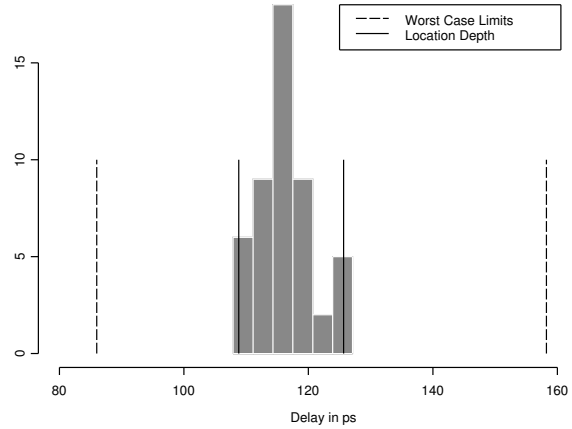


Fig. 10. Simulation results for CMOS ring oscillator delay: Location Depth Corner Model (LDCM) vs. standard worst case.

Figures 10 and 11 contain the histogram for the simulated delay of the ring oscillator. In Figure 10 the standard worst case limits (worst case speed and worst case power, dashed lines) are compared with the limits generated by the Location Depth Corner Model (solid lines). The limits of the LDCM correspond to the 2 extreme delay corners out of all 12 statistical corners. The worst case limits are far outside the range of the delay data whereas the limits of the LDCM represent the statistical range of the delay values by construction.

The simulation results for the ELDCM with different portions ($q = 0.1, 0.2, 0.3, 0.4, 0.5$) are shown in Figure 11. Clearly, increasing the portion enlarges the delay region and provides more robust, but still suitable performance limits.

C. Analog Application - Operational Amplifier Characterization

Since the statistical models are employed within an analog/mixed-signal design environment, a standard CMOS operational amplifier is chosen as an analog validation example. The four characteristics bandwidth (BW),

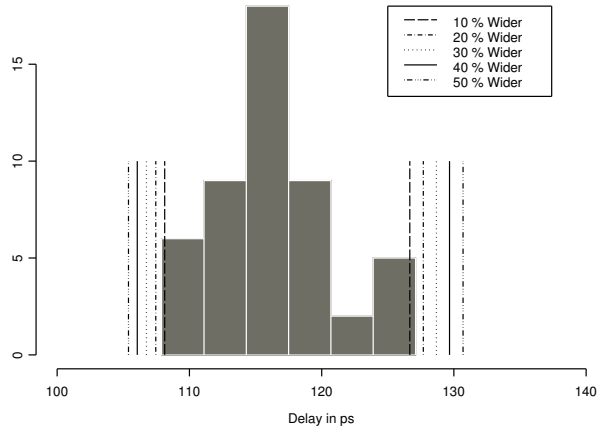


Fig. 11. Simulation results for CMOS ring oscillator delay: Extended Location Depth Corner Method (ELDCM) with different q-values.

open loop gain (OLG), phase margin (PM) and gain bandwidth (GBW) are analyzed for the worst case method, the LDCM and the ELDCM with different q-values. Additionally, a statistically typical wafer w_{st} is selected by the method described in Section III-D.

For a data set of $n = 521$ wafers $m = 14$ e-test parameters per wafer have been analyzed (7 NMOS and 7 PMOS parameters p_e as described in Table I). The LDCM selects $r = 17$ corner wafers (based on $m_d = 10$ search directions) which are also used for the ELDCM. For each corner wafer the values of $k = 16$ SPICE parameters (8 NMOS and 8 PMOS parameters p_s) have been obtained by transformation E2SPICE (7) which uses the extracted SPICE parameter values of the typical wafer and the variation of the corresponding e-test parameters p_e.

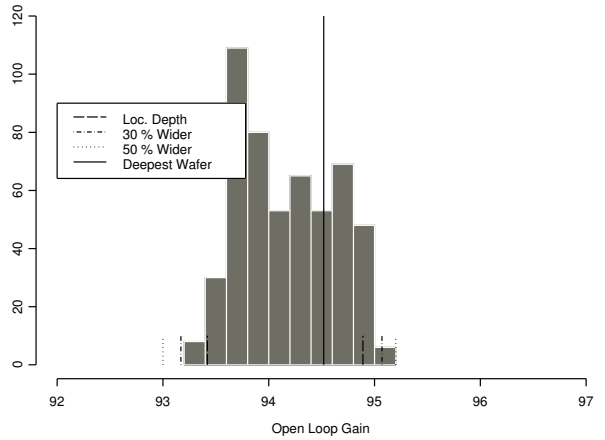


Fig. 12. CMOS OpAmp: Histogram of Open Loop Gain [dB] and simulated corners using LDCM and ELDCM.

The histogram bars in Figure 12 (Figure 13) represent the simulated open loop gain values (phase margin values) of all $n = 521$ wafers where the solid lines represent the values of the statistically typical wafer w_{st} (deepest wafer). The simulated performance ranges of the wafers obtained by the LDCM and the ELDCM ($q = 0.3$ and $q = 0.5$) are indicated as dashed lines.

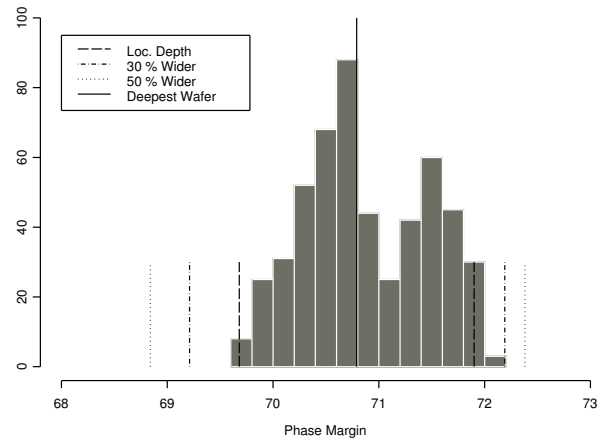


Fig. 13. CMOS OpAmp: Histogram of Phase Margin [deg]. and simulated corners using LDCM and ELDCM.

The performance ranges of all four characteristics with respect to the different models can be found in Table III. *All* represents all $n = 521$ wafers of a given time period, *Loc* the LDCM, *30* (*50*) the ELDCM with a percentage of 30% (50%). *WC* shows the simulated range for the standard worst case method.

The simulation results demonstrate that it is possible to cover the process variation of three analog characteristics by $r = 17$ statistical corners when using the ELDCM method with a 50% safety-margin. Only gain bandwidth could not be completely covered on the left tail. Once again the corner models prove to be more realistic than standard worst case models. The results of the standard worst cases can deviate in both directions: they may be too pessimistic (see CMOS ring oscillator delay - Figure 10), or too optimistic (see CMOS OpAmp open loop gain and bandwidth in Table III). Since only five technological corners are selected by the standard worst case method based on the single device performance IDS this may lead to an over-estimation of the circuit performance range, e.g. for the ring oscillator delay where the IDS variation is of special importance, due to pessimistic parameter ranges (see ring oscillator delay in Figure 10). On the other hand performances like the bandwidth are not covered although they may be important for analog designs. In contrast, the LDCM and the ELDCM do not rely on single device performances, but they search for all corners (i.e. points with location depth less equal one) of the underlying multi-dimensional parameter space. As a consequence, the one-dimensional projections of the established boundary cover the range of the essential characteristics for both analog and digital circuits.

TABLE III
SIMULATION RESULTS FOR CMOS OPERATIONAL AMPLIFIER: BANDWIDTH [HZ], OPEN LOOP GAIN [DB], PHASE MARGIN [DEG] AND GAIN BANDWIDTH [MHZ].

	BW	OLG	PM	GBW
All	205–287	93.2–95.2	69.6–72.1	12.9–16.9
Loc	214–280	93.4–94.9	69.7–71.9	13.9–16.7
30	209–295	93.2–95.1	69.2–72.2	13.7–17.4
50	205–305	93.0–95.2	68.8–72.4	13.6–17.8
WC	207–280	93.5–94.7	67.0–74.5	13.6–16.3

To show the need for a proper selection of the typical wafer in case of process shifts (see Section III-D), we examine the gain bandwidth for the same data as before. But now we include a wafer chosen as typical at an early process stage which remained typical for all parameters except the mobility factor $U0N$ where the value was close to the lower pass/fail limit. A look to the gain bandwidth shows that the value of this wafer is even outside the range of the actual data (left from the minimum, referenced as Typ. Wafer in Figure 14). Clearly, a robust design centering with this wafer value would be impossible. As an alternative we suggest to take the wafer w_{st} with highest location depth (referenced as Deepest Wafer, solid line in Figure 14) determined by the method described in Section III-D. The selected wafer w_{st} represents the median of multivariate data and is well suited for analog design centering.

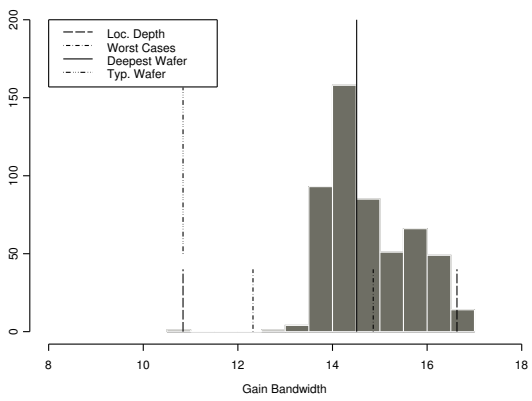


Fig. 14. CMOS OpAmp: Deepest Wafer determination, Histogram of Gain Bandwidth [MHz].

The example clearly demonstrates the need for a consequent re-evaluation of the typical wafer (golden wafer) to enable proper design centering intended for robust designs with high yield.

D. Performance coverage and number of selected corner wafers

The accuracy of corner wafers selected by the ELDCM strongly depends on the number of search directions m_d in the approximate algorithm for the location depth described in Section III-B. A larger number of search directions leads also to a larger number of selected corners. For the data set used in the analog benchmark simulation (total number $n = 521$ wafers) the $m_d = 10$ search directions resulted in $r = 17$ corner wafers. The specific choice was based on an empirical study on the coverage of analog performance specifications. For this we carried out simulations with seven different numbers (2,5,10,12,15,20,25) of search directions yielding (4,9,17,19,25,30,37) corner wafers. We settled for $r = 17$ corner wafers, because a larger number of corner points did not significantly improve the coverage and hence could not compensate the increase in simulation time.

VI. CONCLUSIONS

We introduced two statistical methods to determine simulation models that cover the process variation. The location depth method (LDCM) was used to perform a multivariate ranking of the wafers in the e-test parameter space. To calculate SPICE parameters easily, we defined the linear mapping *e2SPICE* (7) from the e-test parameter space to the SPICE (simulation) parameter space. Owing to the affine invariance of the location depth method and the linearity of the mapping, the ranking does not change when e-test parameters are transformed to SPICE parameters.

With the Location Depth Corner Method, a small set of wafers (between 10 and 30) near the corners of the process could be found. With the Extended Location Depth Corner Method (ELDCM), the simulation region defined by the wafers of the LDCM could be enlarged by adding a safety-margin to the region. The corner models provided by the two methods, allowed us to perform realistic and fast simulations of electrical circuits.

To ensure a convenient generation of the simulation models by the LDCM and the ELDCM, the two models were integrated into an automated SPICE parameter generation flow. To facilitate the use of the LDCM and ELDCM simulation models for the designer, corner definition files have been generated for an easy integration into the Cadence-Affirma^{TM} design framework.

To verify the simulation models obtained with our statistical methods, a representative digital design (Ring Oscillator) and an analog design (Operational Amplifier) have been simulated. The results show that the process variation is correctly described by the simulated range of corner models for both digital and analog designs using a small number of simulation runs (12 to 17).

Another important aspect addressed in this paper was the determination of a statistically typical wafer. The histograms in Section V-C show that because of process shifts it may happen that a typical wafer may not be typical in all parameters. Therefore, a design centering can be facilitated by selecting a wafer with the largest location depth (deepest wafer) as a statistically typical wafer. For a regular validation and update of the statistical models generated, suitable test circuits (process benchmarks) of analog/mixed-signal reference designs (e.g. Ring Oscillators, Operational Amplifiers, Band Gaps etc.) must be

available as process control structures which allow to verify the link between production control parameters and SPICE parameters.

References

[1] K. Singhal and V. Visvanathan, "Statistical device models from worst case files and electrical test data," *IEEE Trans. on Semiconductor Manufacturing*, vol. 12, no. 4, pp. 470–484, November 1999.

[2] C. Marzocca, G. Matarrese, E. Cantatore, F. Corsi, "Relative robustness against process fluctuations of basic building blocks for analog front-end of particle detectors," *Proceedings of the 5th Workshop on Electronics for LHC Experiments, Snowmass, Colorado 20-24, September*, 1999.

[3] J. Purviance and M. D. Meehan, *Yield and Reliability in Microwave Circuit and System Design*, Artech House Publishers, 1993.

[4] R. S. Soin and R. Spence, *Tolerance Design of Electronic Circuits*, Imperial College Press, 1997.

[5] S.M. Kang and A. Dharchoudhury, "Worst-case analysis and optimization of VLSI circuit performances", *IEEE Trans. Computer-Aided Design*, vol. 14, no. 4, pp. 481–492, April 1995.

[6] I. N. Hajj, T. N. Trick, Tat-Kwan Yu, S. M. Kang, "Statistical performance modeling and parametric yield estimation of MOS VLSI", *IEEE Trans. Computer-Aided Design*, vol. CAD-6, no. 6, pp. 1013–1022, Nov. 1987.

[7] D. Stoneking, "Device modeling using non-parametric statistical determination of boundary vectors", *U.S. Patent 5 835 891* , Nov. 1998.

[8] M. Kocher and G. Rappitsch, "Statistical methods for the determination of process corners", *Proceedings of the ISQED 2002, 3rd International Symposium on Quality Electronic Design*, San Jose, March 2002.

[9] Y. Cheng et al., "A physical and scalable I-V model in BSIM3V3 for analog/digital circuit simulation", *IEEE Trans. on Electronic Devices*, vol. 44, no. 5, pp. 277–287, Feb. 1990.

[10] B. Ankele, W. Hölzl and P. O'Leary, "Enhanced MOS parameter extraction and SPICE modelling for mixed signal analogue and digital circuit simulation", *IEEE International Conference on Microelectronic Test Structures*, pp. 133–137, Edinburgh, 1989.

[11] D. Stoneking, "Statistical circuit design and IC-CAP's non-parametric boundary analysis", *Solutions from HP EEsof*, vol. 2, no. 2, pp. 1–13, 1997.

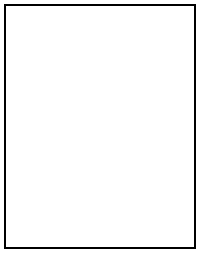
[12] P. J. Rousseeuw and A. Struyf, "Computing location depth and regression depth in higher dimensions", *Statistics and Computing*, vol. 8, pp. 193–203, 1998.

[13] J. W. Tukey, "Mathematics and the picturing of data", *Proceedings of the International Congress of Mathematicians*, pp. 523–531, Vancouver, 1997.

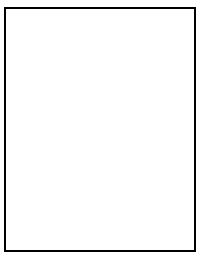
[14] A. Struyf and P. J. Rousseeuw, "High-dimensional computation of the deepest location", *Computational Statistics and Data Analysis*, vol. 34, pp. 415–426, 2000.

[15] "S-PLUS 2000", *Data Analysis Products Division, MathSoft, Inc.*, Seattle, Washington.

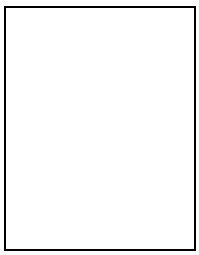
[16] "AffirmaTM Analog Circuit Design Environment User Guide, Product Version 4.4.6" *Cadence Design Systems*, 2002. Washington.



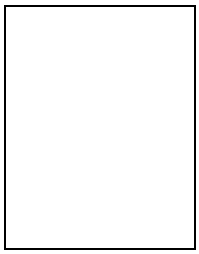
Gerhard Rappitsch received his degree as graduate engineer in Technical Mathematics from the Graz University of Technology (TUG) in 1991 and in 1996 his Ph.D. degree in Technical Sciences from the same university. From 1992 to 1996 he was with the Austrian Science Fund and member of a research team on High Performance Computing and Numerical Methods at the TUG. Since 1997 he is at the Research & Development department of *austriamicrosystems AG* working in the areas of analog circuit simulation, SPICE modeling and design framework integration. A major research area focuses on statistical device modeling for robust analog/mixed-signal design purposes (corner modeling and Monte Carlo methods).



Ehrenfried Seebacher earned a M. Sc. degree in Physics in 1993 at the Graz University of Technology. From 1994 until 1998 he has been working in the R&D Department of *austriamicrosystems AG*, on SPICE modeling of CMOS, BiCMOS and HV CMOS processes. Since 1999 he is the section manager of the Process and Device Characterisation group at *austriamicrosystems AG*. The group is responsible for device modeling, process characterisation, verification run-sets, and SPICE simulator support. His main research areas are compact modeling of MOS transistors (BSIM3V3, BSIM4), bipolar transistors and passive devices.



Michael Kocher received his degree as graduate engineer in Technical Mathematics from the Graz University of Technology in 2000. He has been working as process characterization engineer at *austriamicrosystems AG*, Unterpremstätten, Austria from 2001 to 2002. His research was concentrated on the statistical corner modeling of semiconductor devices and design-framework implementation. 2002 he finished his Ph.D. degree in Technical Sciences at the Institute of Statistics, TUG and is at present working as a statistician at *Standard Life* in Frankfurt/Main, Germany.



Ernst Stadlober studied Technical Mathematics at the Graz University of Technology. Earned a diploma degree and became Univ.-Assistent 1975. Obtained his Ph.D. degree in Technical Sciences at the same university in 1983 and finished his Habilitation 1989. Since 1997 he is Full Professor for Applied Statistics at the Institute of Statistics, TUG. His research topics are random variate generation, stochastic modeling and simulation, biometrics and industrial statistics. He has published more than 40 papers in international journals and conference proceedings.